REMARKS

Claims 1-6 are pending. Paragraph 57 of the specification has been amended to include a basic reference to Figure 7. No new matter has been added.

The Examiner is invited to call the undersigned attorney to answer any questions or to discuss steps necessary for placing the application in condition for allowance.

Respectfully submitted,

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Addendum
Marked-Up Versions of Specification and Abstract
Showing Insertions and Deletions

[0057] It should be noted that, in a case where the AGC operation is stopped and the signal states of each section are initialized, the state of the signal applied to the reset terminal RESET is varied from "H" to "L". Here, a specific example of the aforementioned discrete analog drive will be described. In Figs. 3 and 6, plural values of, for example, 1V, 2V and 3V are set with respect to the voltages (drive signal VAGC) applied to the transistors MP0 and MN0. That is, in Figs. 3 and 6, they are connected in parallel to plural level hysteresis comparators CMP1, CMP2 and CMP3, and RS flip-flop circuits RSFF1, RSFF2 and RSFF3 are connected in correspondence to the hysteresis comparators CMP1 to CMP3 as shown in Fig. 7, so that a plural level configuration is formed. The output terminals of the RS flip-flop circuits RSFF1 to RSFF3 are connected to a decoder. The drive signal VAGC is outputted from the decoder.